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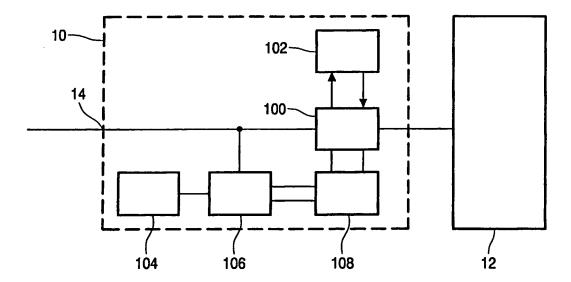
- (74) Agent: DULJVESTIJN, Adrianus, J.; Philips Intellectual Property & Standards, Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).
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[Continued on next page]

(54) Title: DATA PROCESSING APPARATUS THAT PROCESSES INCOMING BITS



(57) Abstract: A data processing apparatus receives a communication signal that contains temporally successive bits. A programmable processor circuit executes a plurality of series of programmed instructions for operations such as parity checking, each at a time of reception of a respective one of the bits. The processor circuit suspends operation each time after executing a respective one of the series of instructions. A synchronization circuit triggers execution of respective ones of the series, each time at the time of reception of the respective one of the bits, and, except for a last one of the series, prior to reception of one or more later bits that contribute to the data word.



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According to	o International Patent Classification (IPC) or to both national class	fication and IPC		
B. FIELDS	SEARCHED		· · · · · · · · · · · · · · · · · · ·	
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° Special ca	ategories of cited documents:	T later document pu	blished after the International fil	ing date
consider of the constant of th	ent which may throw doubts on priority claim(s) or	cited to understa invention "X" document of parti- cannot be consid	nd not in conflict with the applicand the principle or theory under cular relevance; the claimed inviered novel or cannot be considered by the step when the document is in the course of the course o	lying the ention ered to
which citation other	is cited to establish the publication date of another n or other special reason (as specified) ent referring to an oral disclosure, use, exhibition or means ent published prior to the international filing date but	cannot be considered to come the considered to considered the constant in the	cular relevance; the claimed inviered to involve an inventive ste bined with one or more other subination being obvious to a pen	p when the uch docu-
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